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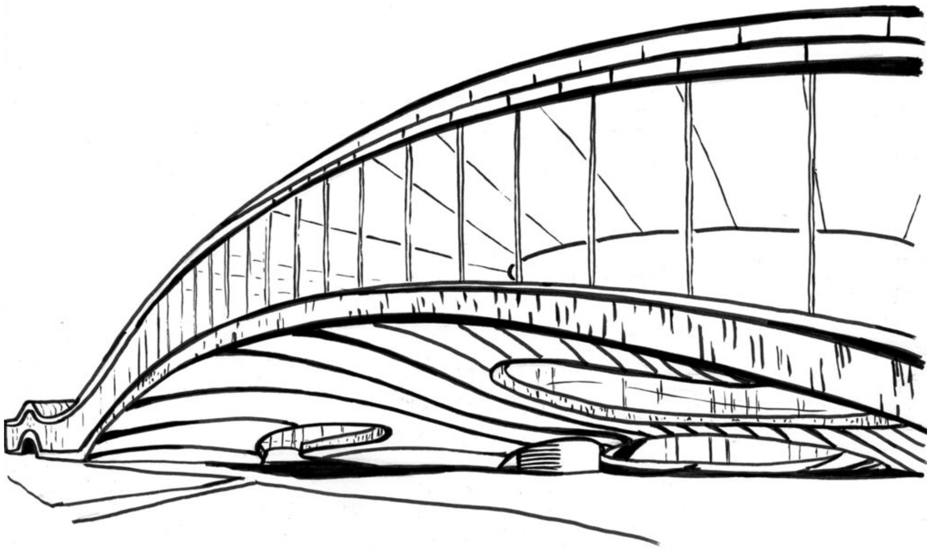

Using ZDDs in the mapping of quantum circuits

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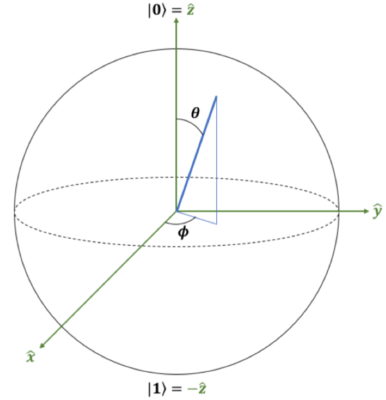
Quantum Computing Basics

- A qubit represents information as a combination of $|0\rangle = \begin{bmatrix}1\\0\end{bmatrix}, |1\rangle = \begin{bmatrix}0\\1\end{bmatrix}$:

$$|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$$

- Superposition allows an infinite number of states of form: $|\alpha|^2 + |\beta|^2 = 1$
- Measurement causes qubit state to collapse to a basis state
- Transformations of quantum information represented by transfer matrix, $\mathbf{U}$
- Qubit operations can be decomposed into $R_x(\theta), R_y(\theta), R_z(\theta)$ rotations

Bloch Sphere



$$|\Psi(t)\rangle = \mathbf{U}|\Psi(t_o)\rangle$$

Qubit(s) State

QC Gate/Operation

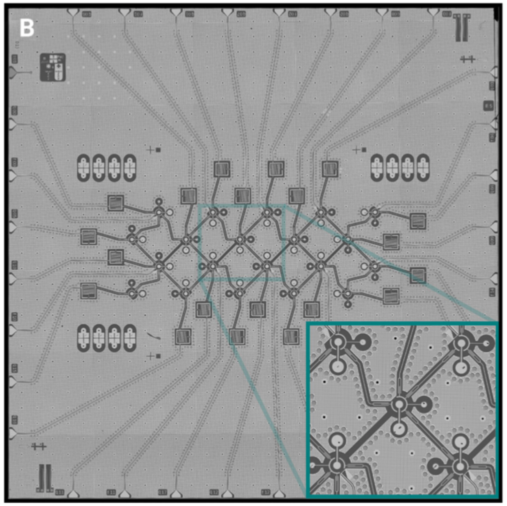
$$R_x(\theta) \equiv e^{-i\frac{\theta}{2}X} = \cos\frac{\theta}{2}I - i\sin\frac{\theta}{2}X = \begin{bmatrix}\cos\frac{\theta}{2} & -i\sin\frac{\theta}{2}\\ -i\sin\frac{\theta}{2} & \cos\frac{\theta}{2}\end{bmatrix}$$

$$R_y(\theta) \equiv e^{-i\frac{\theta}{2}Y} = \cos\frac{\theta}{2}I - i\sin\frac{\theta}{2}Y = \begin{bmatrix}\cos\frac{\theta}{2} & -\sin\frac{\theta}{2}\\ \sin\frac{\theta}{2} & \cos\frac{\theta}{2}\end{bmatrix}$$

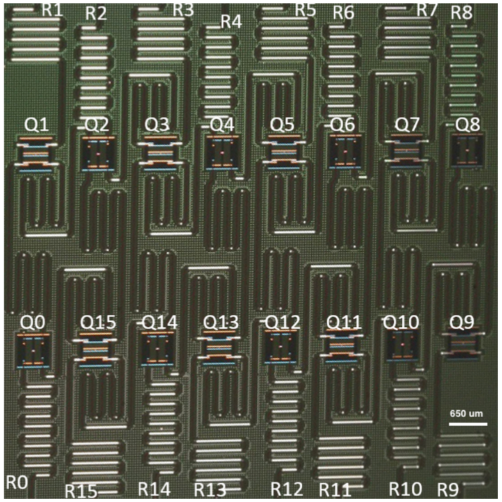
$$R_z(\theta) \equiv e^{-i\frac{\theta}{2}Z} = \cos\frac{\theta}{2}I - i\sin\frac{\theta}{2}Z = \begin{bmatrix}e^{-i\theta/2} & 0\\ 0 & e^{i\theta/2}\end{bmatrix}$$

Quantum Information Realization

- Quantum Computing currently with Noisy Intermediate-Scale Quantum (NISQ) technology
- Some platforms based on similar technology
  - Ex. superconducting/ semiconductor circuits
- Different native operators and topologies
  - IBM : $\mathrm{CNOT}, \mathrm{U}(x, y, z)$
  - Rigetti : $\mathrm{CZ}, R_z(\theta), R_x\left(k * \frac{\pi}{2}\right)$



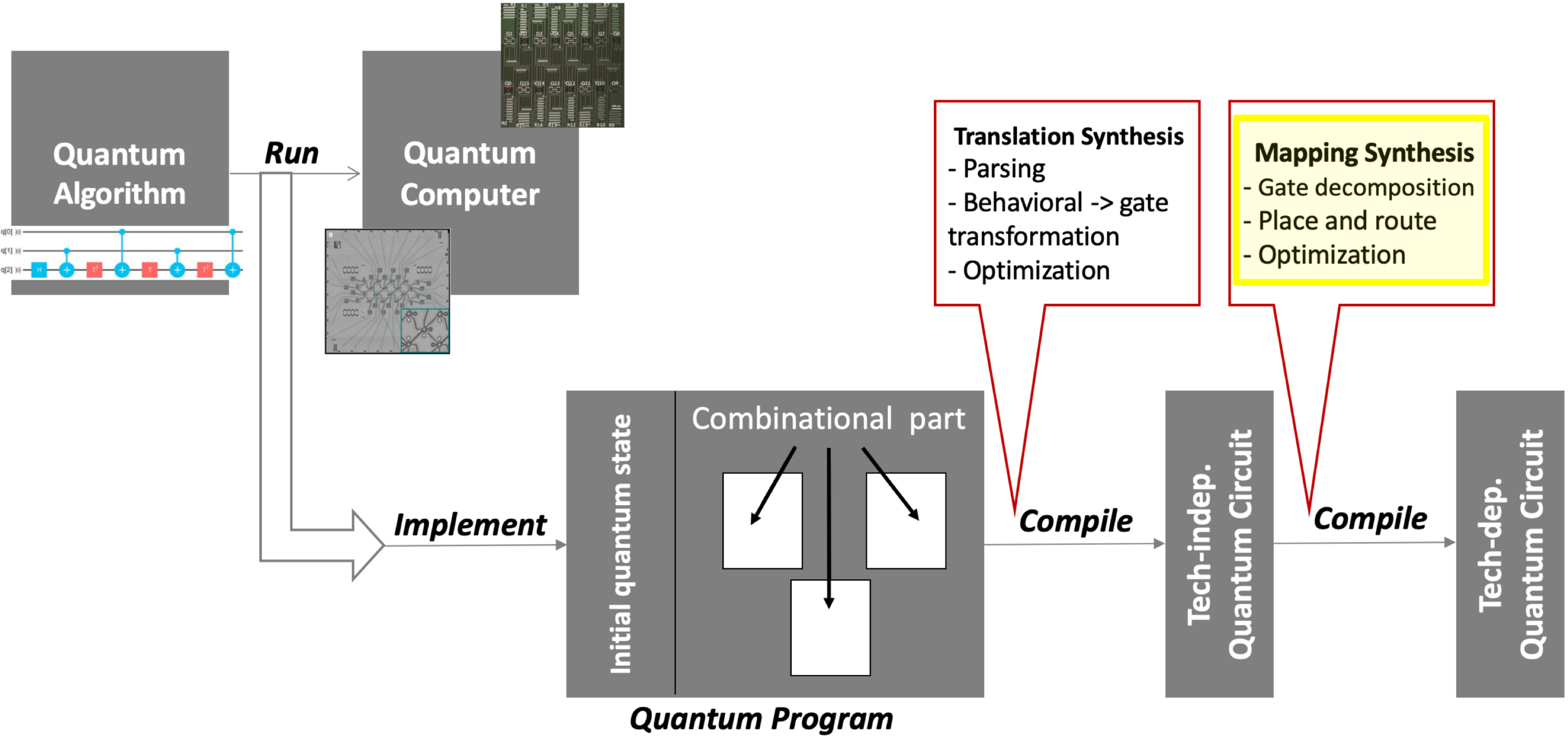
Rigetti Device



IBM Device

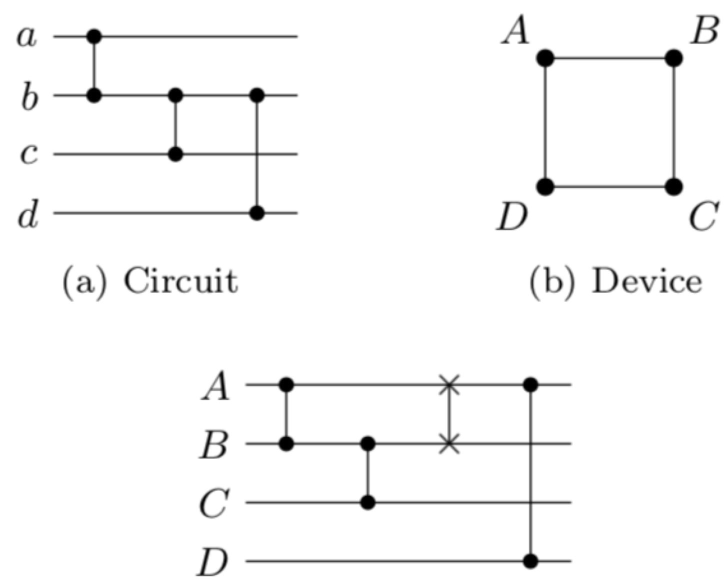
Images: https://github.com/QISKit/ibmqx-backend-information/tree/master/backends, https://arxiv.org/pdf/1712.05771.pdf

Problem Definition



The Mapping Problem

- Generalized quantum algorithms are not technology-ready
- Need to determine mapping from pseudo (V) → physical (P) qubits while keeping in mind:
  1. Number of maps available
  2. Limitations with respect to gate volume and gate depth
- Approach assumes ***decomposition*** has already taken place



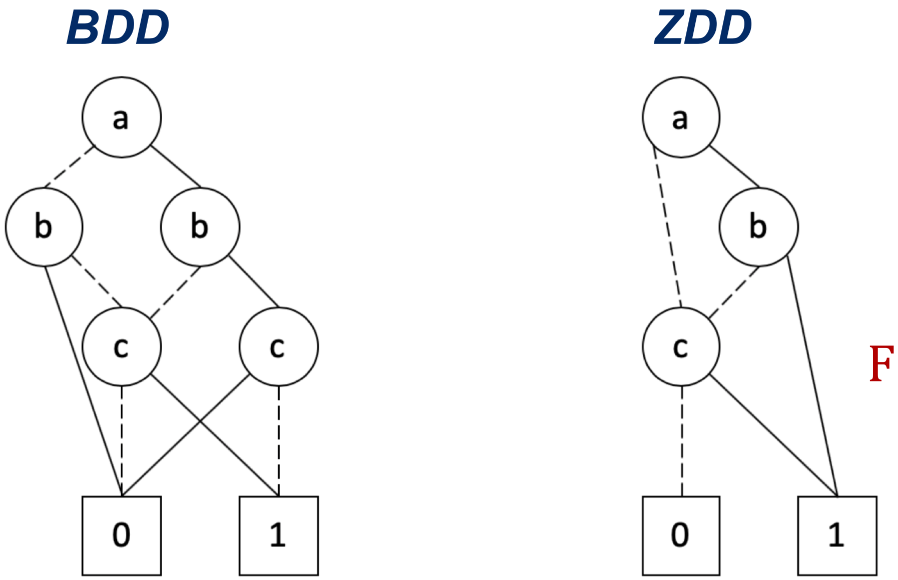
(a) Circuit (b) Device

(c) Mapped circuit

Simple circuit and device

Zero-suppressed Decision Diagrams (ZDD)

- ***Modified*** reduction rules compared to BDD
  - Eliminate all nodes where 1-edge points to 0
  - Share all equivalent subgraphs
  - Keep nodes with two edges pointing to same node
- Ideal for representing sparse sets



$\{\{a,b\},\{a,c\},\{c\}\} \rightarrow$
$F = ab\bar{c} + a\bar{b}c + \bar{a}\bar{b}c$

Representations for the set of subsets {{a,b},{a,c},{c}}

Key Set Operations

- Union : $f \cup g = \{\alpha \mid \alpha \in f \ or \ \alpha \in g\}$
- Intersection : $f \cap g = \{\alpha \mid \alpha \in f \ and \ \alpha \in g\}$
- Difference : $f \backslash g = \{\alpha \mid \alpha \in f \ and \ \alpha \notin g\}$
- Join : $f \sqcup g = \{\alpha \cup \beta \mid a \in f \ and \ \beta \in g\}$
- Meet : $f \sqcap g = \{\alpha \cap \beta \mid a \in f \ and \ \beta \in g\}$
- Nonsupersets : $f \searrow g = \{\alpha \in f \mid \beta \in g \ implies \ \alpha \not\supseteq \beta\}$
- Choose : $\binom{f}{k} = select \ k \ items \ from \ f$

Example 1: Set Operations

$$a = \{\{1,2,3\}, \{3,4\}, \{5\}\} \; ; b = \{\{0,2,3\}, \{3,4\}, \{6\}\}$$

- Union : $a \cup b = \{\{1,2,3\}, \{3,4\}, \{5\}, \{0,2,3\}, \{3,4\}, \{6\}\}$
- Intersection : $a \cap b = \{\{3,4\}\}$
- Difference : $a \backslash b = \{\{1,2,3\}, \{5\}\}$
- Join : $a \sqcup b =$ $\{\{0,1,2,3\}, \{1,2,3,4\}, \{1,2,3,6\}, \{0,2,3,4\}, \{3,4\}, \{3,4,6\}, \{0,2,3,5\}, \{3,4,5\}, \{5,6\}\}$
- Meet : $a \sqcap b = \{\{2,3\}, \{3\}, \{3,4\}\}$
- Nonsupersets : $a \searrow b = \{\{1,2,3\}, \{5\}\}$

Set Operations for ZDDs during Mapping

$V = pseudo\ qubits$
$P = physical\ qubits$
$\mathrm{E} = device\ edges$
$\mathrm{G} = circuit\ gates$

$$from(v) = \bigcup_{p \in P} \epsilon_{vp}$$

$$to(p) = \bigcup_{v \in V} \epsilon_{vp}$$

$$valid = \bigcup_{\{p,q\} \in E} to(p) \sqcup to(q)$$

$$bad = \bigcup_{v \in V} \binom{from(v)}{2} \cup \bigcup_{p \in P} \binom{to(p)}{2}$$

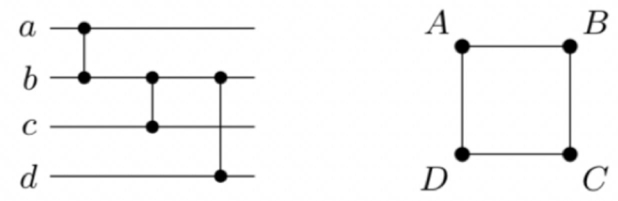
$$map(i) = (from(v) \sqcup from(w)) \cap valid; \ \ where\ g_i = \{v, w\}$$

$$mappings(map_i, map_{i+1}) = (map(i) \sqcup map(i+1)) \searrow bad.$$

$$edges(p) = \bigcup \{\epsilon_e \mid e \in E \text{ s.t. } p \in e\}$$

$$layers = \wp \searrow \bigcup_{p \in P} \binom{edges(p)}{2}$$

Simple circuit and device



(a) Circuit (b) Device

$V = \{a, b, c, d\} \quad P = \{A, B, C, D\}$

$E = \{\{A, B\}, \{B, C\}, \{C, D\}, \{D, A\}\}$

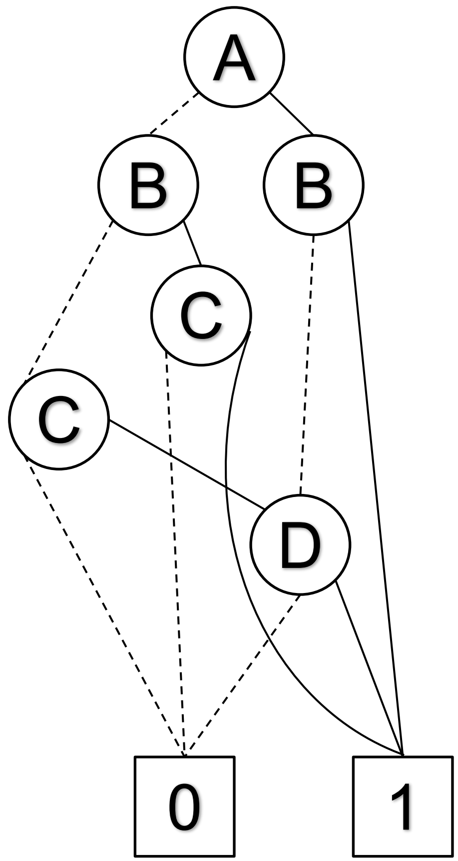
$G = \{g_1, g_2, g_3\} = \{\{a, b\}, \{b, c\}, \{b, d\}\}$

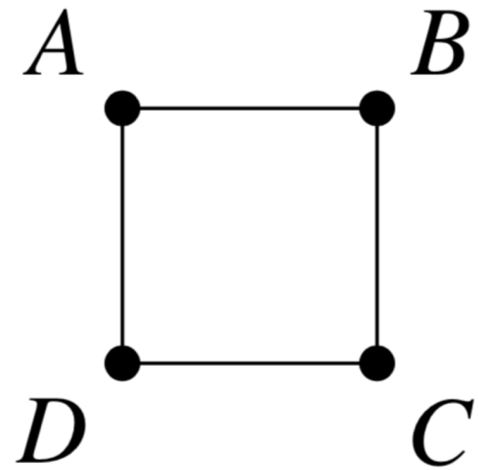
$from(v) = \{\{v, A\}, \{v, B\}, \{v, C\}, \{v, D\}\}$

$to(p) = \{\{a, p\}, \{b, p\}, \{c, p\}, \{d, p\}\}$

Example 2: Edges ZDD

$$E = \{\{A, B\}, \{B, C\}, \{C, D\}, \{D, A\}\}$$

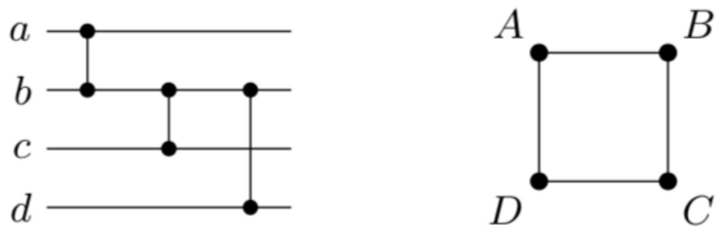




Example 3: Mapping Two Consecutive Gates

$$g_i = \{v, w\}$$

$$map(i) = (from(v) \sqcup from(w)) \cap valid$$



(a) Circuit (b) Device

$$g_1 = \{a, b\} \qquad map(1) = \{\{aA, bB\}, \{aB, bC\}, \{aC, bD\}, \{aD, bA\} \{aB, bA\}, \{aC, bB\}, \{aD, bC\}, \{aA, bD\}\}$$

$$g_2 = \{b, c\} \qquad map(2) = \{\{bA, cB\}, \{bB, cC\}, \{bC, cD\}, \{bD, cA\} \{bB, cA\}, \{bC, cB\}, \{bD, cC\}, \{bA, cD\}\}$$

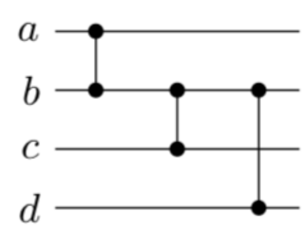
$$(map(i) \sqcup map(i+1)) \searrow bad \qquad \{\{aA, bB, cC\}, \{aB, bC, cD\}, \{aC, bD, cA\}, \{aD, bA, cB\}, \{aA, bD, cC\}, \{aB, bA, cD\}, \{aC, bB, cA\}, \{aD, bC, cB\}\}$$

Example 4: Calculate Layers

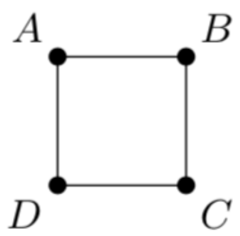
$$edges(p) = \bigcup\{\varepsilon_e \mid e \in E \text{ s.t. } p \in e\}$$

$$edges(A) = \{\{AB\},\{AD\}\}, \quad edges(C) = \{\{BC\},\{CD\}\},$$

$$edges(B) = \{\{AB\},\{BC\}\}, \quad edges(D) = \{\{CD\},\{AD\}\}.$$



(a) Circuit



(b) Device

$$layers = \wp \searrow \bigcup_{p \in P} \binom{edges(p)}{2}$$

$$\bigcup_{p \in P} \binom{edges(p)}{2} = \{\{AB,AD\},\{AB,BC\},\{BC,CD\},\{CD,AD\}\}$$

$$\wp = \{\emptyset,\{AB\},\{BC\},\{CD\},\{AD\},\{AB,BC\},\{AB,CD\},\{AB,AD\},\{BC,CD\},\{BC,AD\},$$
$$\{CD,AD\},\{AB,BC,CD\},\{AB,BC,AD\},\{AB,CD,AD\},\{BC,CD,AD\},\{AB,BC,CD,AD\}\}$$

$$layers = \{\emptyset,\{AB\},\{BC\},\{CD\},\{AD\},\{AB,CD\},\{BC,AD\}\}$$

ZDD Mapping Algorithm

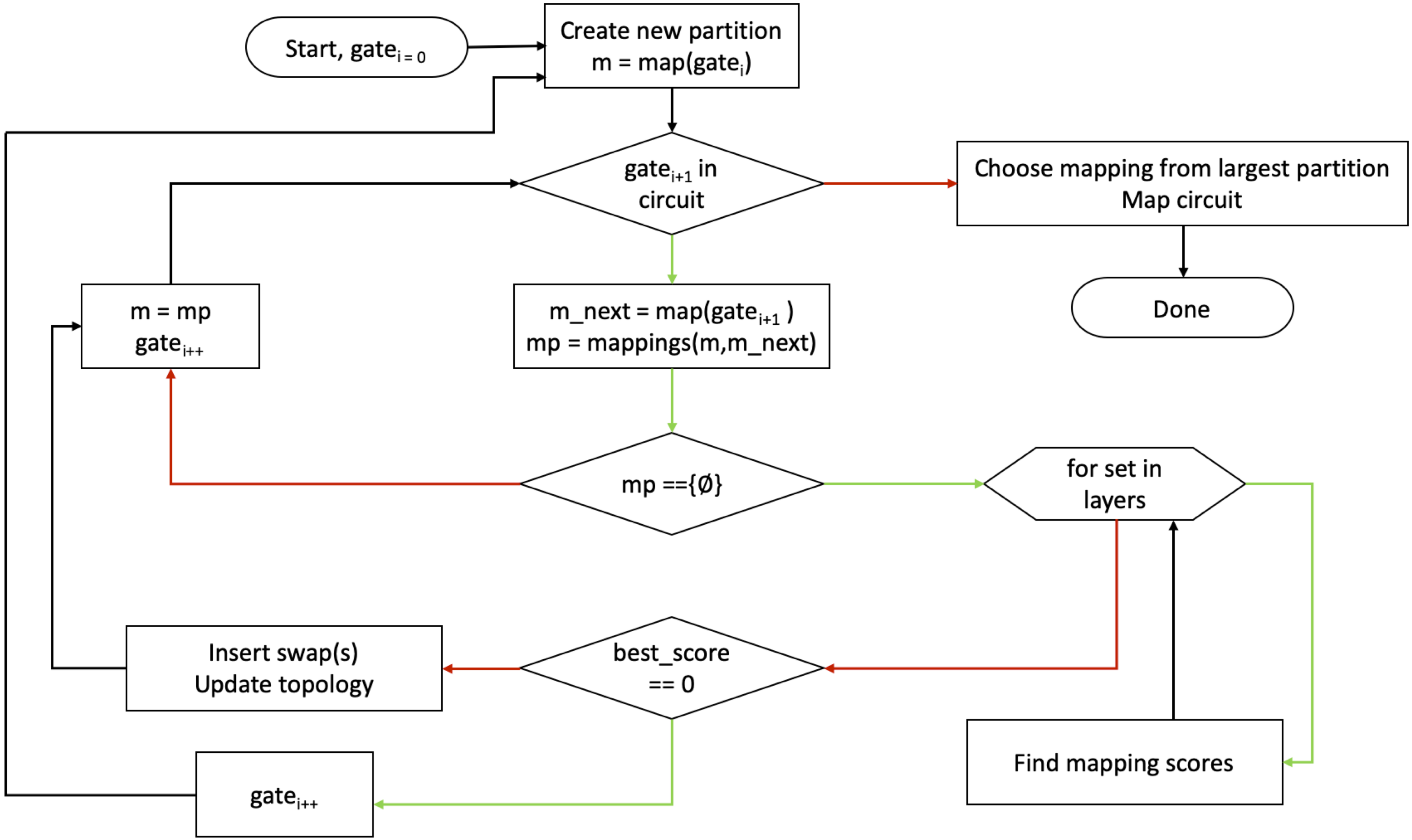
- Use ZDD to represent available maps for pseudo qubits → physical qubits
  - Groups of gates covered by a set of mappings are a ***partition***
- ZDD represents layers of SWAP operations that can execute in parallel
  - Expand partition by selecting optimized SWAP operations from *layers*
- Determine largest partition that can be connected with parallel swap operations
- Mapping from largest partition used to map circuit

Data: Gate sequence $g_1, \ldots, g_k$, and device (P, E)
Result: partitions G_j with begin and end indexes b_j, e_j; all possible mappings Φ_j
Set $j \leftarrow 1$, $b_j \leftarrow 1$, $m \leftarrow map(1)$;
for $i = 2, \ldots, k$ **do**
  Set $m' \leftarrow (m \sqcup map(i)) \searrow bad$;
  if $m' = \emptyset$ **then**
    for *layer in layers* **do**
      calculate scores;
    end
    if *max score* $\neq 0$ **then**
      insert SWAP circuit;
      update topology;
      Set $m(\text{max score})' \leftarrow (m \sqcup map(i)) \searrow bad$;
      Set $m \leftarrow m'$;
    else
      Set $e_j \leftarrow i - 1$, $\Phi_j \leftarrow m$;
      Set $j \leftarrow j + 1$, $b_j \leftarrow i$, $m \leftarrow map(i)$;
    end
  else
    Set $m \leftarrow m'$;
  end
end
Set $e_j \leftarrow k$, $\Phi_j \leftarrow m$;

Algorithm 1: Find maximal partitions

$$score = (A\alpha + B\beta)\frac{\gamma}{C}$$

$\alpha = depth\ weight$
$A = depth\ count$
$\beta = map\ weight$
$B = map\ count$
$\gamma = SWAP\ weight$
$C = SWAP\ count$


Start, gate$_{i=0}$
Create new partition
m = map(gate$_i$)
gate$_{i+1}$ in circuit
Choose mapping from largest partition
Map circuit
Done
m = mp
gate$_{i++}$
m_next = map(gate$_{i+1}$)
mp = mappings(m,m_next)
mp =={Ø}
for set in layers
Insert swap(s)
Update topology
best_score == 0
Find mapping scores
gate$_{i++}$

ZDDs in the Quantum Compilation Flow

ZDD mapping techniques used in larger logic synthesis flow:

1. Decomposition of operators into one- and two-qubit primitives
2. Perform qubit mapping with maximal partition found from ZDD mapping algorithm
3. Apply technology platform's compilation tools for transformations/optimizations for native gate library

Experimental Results

- Ring topologies for IBM/Rigetti quantum computers targeted
- Benchmarks ranged 5 to 15 qubits
- Methods assessed with:
  - Gate depth
  - Gate volume
  - 2q gate count
- https://github.com/knsmith/zdd_mapping_experiments

Benchmark Name	No. Qubits		Original ZDD Mapped	Original Rigetti Compiled	Original IBM Compiled	ZDD Mapped/ Rigetti Compiled	ZDD Mapped/ IBM Compiled
barenco_tof_3	5	*depth:*	64	118	62	98 *(-16.95%)*	84 *(+35.48%)*
		vol.:	95	446	180	221 *(-50.45%)*	165 *(-8.33%)*
		2q gates:	73	68	67	58 *(-14.71%)*	63 *(-5.97%)*
barenco_tof_4	7	*depth:*	94	230	131	155 *(-32.6%)*	130 *(-0.76%)*
		vol:	190	763	462	449 *(-41.15%)*	335 *(-27.49%)*
		2q gates:	152	123	177	117 *(-4.88%)*	132 *(-25.42%)*
barenco_tof_5	9	*depth:*	94	231	121	155 *(-32.9%)*	130 *(+7.44%)*
		vol.:	285	1136	528	682 *(-39.96%)*	505 *(-4.36%)*
		2q gates:	231	184	201	177 *(-3.8%)*	201 *(+0%)*
gf2^4_mult	12	*depth:*	46	337	251	361 *(+7.12%)*	354 *(+41.03%)*
		vol:	232	2319	1450	2593 *(+11.82%)*	1511 *(+4.21%)*
		2q gates:	145	363	557	430 *(+18.46%)*	587 *(+5.39%)*
gf2^5_mult	15	*depth:*	64	422	259	504 *(+19.43%)*	342 *(+32.05%)*
		vol:	363	3747	2212	4510 *(+20.36%)*	2351 *(+6.28%)*
		2q gates:	230	596	842	775 *(+30.03 %)*	910 *(+8.07%)*
grover_5	9	*depth:*	210	968	989	872 *(-9.92%)*	552 *(-44.19%)*
		vol:	777	4857	2909	4484 *(-7.68%)*	2590 *(-10.97%)*
		2q gates:	441	781	1096	739 *(-5.38%)*	1011 *(-7.76%)*
hwb6	7	*depth:*	113	449	269	432 *(-3.79%)*	290 *(+7.81 %)*
		vol:	303	2032	1049	2027 *(-0.25%)*	1101 *(+4.96%)*
		2q gates:	185	332	404	338 *(+1.81%)*	422 *(+4.46%)*
mod_mult _55	9	*depth:*	49	189	123	177 *(-6.35 %)*	144 *(+17.07 %)*
		vol:	155	978	500	850 *(-13.09 %)*	469 *(-6.2%)*
		2q gates:	88	151	193	143 *(-5.3 %)*	176 *(-8.81%)*
mod_5 _4	5	*depth:*	60	115	94	95 *(-17.4%)*	92 *(-2.13%)*
		vol:	121	459	229	308 *(-32.9%)*	239 *(+4.37%)*
		2q gates:	98	73	88	79 *(+8.21%)*	92 *(+4.55%)*
qft _4	5	*depth:*	142	162	155	137 *(-15.43%)*	105 *(-32.26%)*
		vol:	247	447	322	433 *(-3.13%)*	293 *(-9.01%)*
		2q gates:	120	79	126	92 *(+16.46%)*	114 *(-9.52%)*
tof_3	5	*depth:*	39	98	62	72 *(-26.53%)*	61 *(-1.61%)*
		vol.:	75	309	145	195 *(-36.89%)*	135 *(-6.9%)*
		2q gates:	54	47	53	45 *(-4.26%)*	52 *(-1.89%)*
tof _4	7	*depth:*	46	117	98	88 *(-24.79%)*	62 *(-36.73%)*
		vol:	125	505	326	327 *(-35.25%)*	218*(-33.12%)*
		2q gates:	92	80	121	75 *(-6.25%)*	84 *(-30.58%)*
tof _5	9	*depth:*	46	118	68	89 *(-24.58%)*	62 *(-8.82%)*
		vol:	175	707	335	459 *(-35.08%)*	308 *(-8.06%)*
		2q gates:	130	112	132	106 *(-5.36%)*	118 *(-10.61%)*
vbe _adder _3	10	*depth:*	67	216	165	197 *(-8.8%)*	232 *(+40.61%)*
		vol:	162	1244	765	1131 *(-9.08%)*	835 *(+9.15%)*
		2q gates:	122	190	294	195 *(+2.63%)*	329 *(+11.9%)*

Thank you!